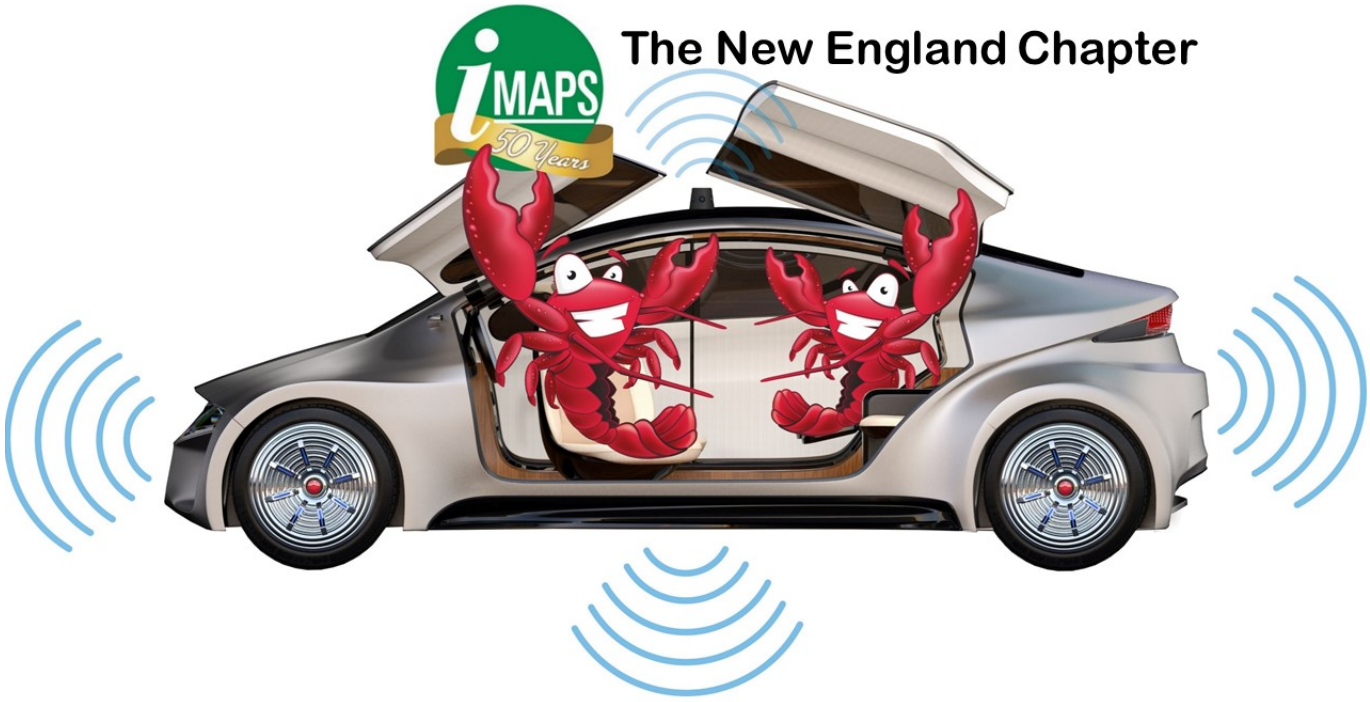
iMAPS New England

45th Symposium & Expo

Technical Program

Tuesday May 1st 2018

Boxboro Regency Hotel
Boxborough, MA



"Into the Future Autonomously"

Jon Medernach

IMAPS NE
Chapter President

Lee Levine & Dave Saums

IMAPS NE
Symposium Technical
Chairs

*i*MAPS New England - May 1st, 2018

Welcome all to the 45th Annual *i*MAPS New England Symposium and Expo. This one day event with more than thirty technical presentations and over 50 vendors is the largest chapter held event in the world ! It is all thanks to a group of dedicated volunteers that have work very hard over the past year to make this a success.

A special Thank You to Lee Levine and Dave Saums our Technical Co- Chairs for their leadership and tenacity and to Dmitry Marchenko for his help and guidance. We are offering Sessions on MEMS, Printed Electronics, RF and Microwave, Novel Packaging, Interconnect Technology and Photonics. The session chairs have put together an outstanding collection of topics for this year's event.

We are also putting more focus on the Poster Session for this event and special thanks to Dipak Sangupta, Harvey Smith, and Dave Saums for their efforts in this area. As our floor space and technical session slots are limited a Poster is a great way to get your information out to our crowd.

Our Keynote could not be more topical, Sensing Technologies for an Autonomous Tomorrow ! Chris Jacobs, a Vice President at Analog Devices, will present "*Giving Autonomous Vehicles the Critical Senses of Sight and Felling"*! My thanks to Chris and to Analog Devices for supporting our event.

This event would not be possible without the support of our Sponsors:

2018 Symposium Gold Sponsors

I want to thank those sponsors and urge everyone to support those businesses.

Finally, I would like to thank the Executive Committee for their work on making this symposium a success. There are untold details to putting on an event like this and it takes a small army to put it all together. From setting up the venue and registration to publishing the proceedings there is a great deal of effort that goes into this day, thank you all for your support.

Jonathan Medernach

President, *i*MAPS New England Chapter

Symposium Technical Chairs' Welcome Letter

Lee Levine

We would like to welcome everyone to the 45th Annual New England *i*MAPS Symposium! Thanks to all the Session Chairs, we've compiled an engaging program of technical talks on many of today's hot topics that will peak the interest of every Attendee. We hope you take full advantage of the opportunity to interact with the speakers and each other in a learning environment that's only available at this unique one-day symposium. Below is a brief summary to help you on your way and don't forget to spend time in the exhibit hall, because after all, without the support of the exhibitors, this day wouldn't be possible. Enjoy!!!

Dave Saums

Photonics & Optoelectronics Packaging: Mid-Infrared chemical sensors, quantum dot and other advanced lasers, advanced manufacturing, and prototyping of photonic devices will all be featured in this session on Optoelectronic packaging. Speakers from MIT, UMass Lowell, IPG Photonics, and MRSI will discuss their newest products and research in the field of Photonic and Optoelectronic devices.

MEMS: This session covers the latest advancements in MEMS and Nano System packaging. Nanomaterial-based smart patches for low-cost MEMS packaging, Si3N4 tuning fork cavity transducers, high-density interposers and ion-milling for MEMs manufacturing will be included in this session covering the challenges of manufacturing micro-mechanical based devices. State of the art techniques and device designs will be shown. Talks by Draper, Worcester Polytechnic, Flex Boston, Innovation Center, and Ion Beam Milling will be featured.

RF & Microwave - Innovations and Emerging Technologies: 5G telecommunications, RF in automotive applications, phase-noise and packaging role in RF devices will all be featured in this session. Analog Devices, Vishay, i3 Microsystems, Holzworth Instrumentation, Dessault Systems, and Intercept Technology/Liberty Packaging will all provide their views on the latest techniques.

Novel Packaging: Novel packaging for medical applications is all about sensors and wearables. Both a wearable vital signs monitor and an implantable wireless neuro stimulator will be featured. Fabrication of a liquid crystal sensor module will be described. MST, Creative Materials, Exceet, Draper and Netzsch will present an exciting session on state of the art electronic packaging for medical applications.

Interconnects: This year the interconnects session will have papers on die attach, wire bonding and plasma cleaning, all back end of the line processes. The die attach papers will discuss both a new nano-material and characterization of die attach cure. The wire bond papers will include a tutorial on the effect of ultrasonics on the welding process and copper heavy wire wedge bonding. The plasma paper will discuss plasma cleaning prior to conformal coating. Papers will be by Netzsch Instruments, UMass Lowell, Process Solutions, Paderborn University (Hesse Mechatronics), and NanoBio Systems.

Printed Electronics: Printed electronics is one of the most rapidly growing segments of our industry. This year five of the six presentations will focus on the printing of additive metallic elements for both structural and electrical conductivity. Printing metals is a leading-edge technology for both wearables and 3-D structures and this year's talks will be from cutting edge companies such as MIT, Draper, RIT, UTRC, Ten Tech LLC, and Analog Devices.

Interactive Poster Session: This year the competition in student papers is really heating up with $2000 dollars in prizes going to the winners (split between poster and oral presenters) and 16 participants in the poster session! Topics include Printable and Wearable Electronics, FEM, Reliability and Optoelectronics. These students and experts are our future, so please set aside some time to go and talk with each of them to learn what's new on the horizon. Their enthusiasm and interests may be a perfect fit for your organization. Let them show you their work.

Kind Regards,

Lee Levine — Dave Saums

2018 *i*MAPS New England Symposium Technical Chairs

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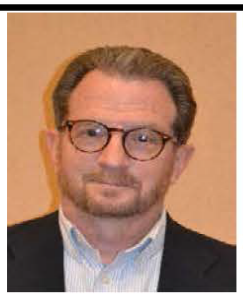

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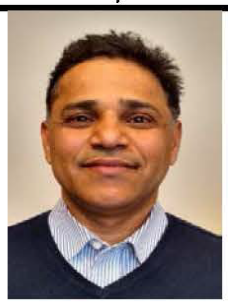

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Keynote Lunch Address

"Sensing Technologies for an Autonomous Tomorrow"

Presented by Chris Jacobs

Vice President, Autonomous Transportation & Automotive Safety

– Analog Devices –

Email: Chris_Jacobs@comcast.net

12:15 – Exhibit Hall

Keynote Abstract:

Chris Jacobs

The future of autonomous transport is upon us. In order to provide safe, reliable transport for all, it is essential to have the most accurate, real time 3D map around the vehicle. The 360 degree safety shield created using RADAR, LIDAR, cameras, and IMUs make up the perception sensor suite that is the foundation for making this a reality. Data from high performance imaging RADAR, LIDAR, and cameras are fused together giving the vehicle it's sense of sight, whereas the IMU gives the vehicle a sense of feeling, while also ensuring it maintains its heading. High performance system sensor solutions from Analog Devices to address these key challenges in autonomous transport will be presented.

Biography:

Chris Jacobs joined ADI in 1995. During his tenure at Analog Devices, Jacobs has held a number of design engineering, design management, and business leadership positions on the Consumer, Communications, Industrial and Automotive teams. Chris Jacobs is currently the Vice President of the Autonomous Transportation & Safety business unit at Analog Devices. Prior to this, Jacobs was the General Manager of Automotive Safety, Product and Technology Director of Precision Converters and the Product Line Director of High Speed Converts & Isolation Products.

Chris earned his Bachelor of Science Degree in Computer Engineering from Clarkson University, a Master of Science in Electrical Engineering from Northeastern University and a Master of Business Administration from Boston College.

45th Annual Symposium - Tuesday May 1st, 2018

Technical Program - Quick Guide

	Session		Room	Chairs	# Papers
Sessions 8:30 – 11:30 AM					
Morning	A:	MEMS	Colonial	Stephen Bart Rick Morrison	6
	B:	Printed Electronics	Cotillion	Greg Fritz Craig Armiento	6
	C:	RF and Microwave - Innovations & Emerging Technologies	Seminar	Tom Terlizzi Chandra Gupta	6
	G:	Interactive Posters (all day)	Exhibit Hall Presenters: 2:00 – 4:00 PM	Dipak Sengupta Harvey Smith Dave Saums	16
Lunch Break – Exhibit Hall – 11:45AM – 1:15PM					

Sessions 1:00 – 3:30 PM					
Afternoon	D:	Novel Packaging Applications	Colonial	Caroline Bjune Mohammed Wasef	5
	E:	Interconnects	Cotillion	Mike McKeown William Boyce	5
	F:	Photonics & Optoelectronics Packaging	Seminar	Yi Qian Jin Li	5

Exhibit Hall Open 9:00AM – 4:30PM

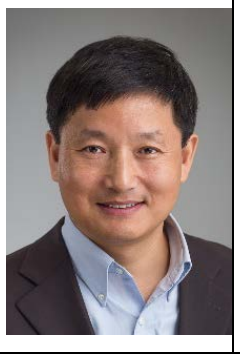
45th Annual Symposium - Tuesday May 1st 2018
Morning Technical Program – Session Chairs

Session		Chair		Chair	
A:	**MEMS**	**Stephen Bart** **Dir. Environmental Sensing** **TDK / InvenSense SSBC** 857-268-4361 sbart@invensense.com		**Rick Morrison** **Engineering Mgr.** **Draper** 617-258-3420 rmorrison@draper.com	
B:	**Printed Electronics**	**Greg Fritz** **Staff Material Scientist** **Draper** 617-258-2563 gfritz@draper.com		**Craig Armiento** **Prof. Printed Electronics Research Collaborative (PERC)** **UMass Lowell** 978-934-3395 Craig_Armiento@uml.edu	
C:	**RF and Microwave: Innovations & Emerging Technologies**	**Tom Terlizzi** **Vice President** **GM Systems LLC** 631-269-3820 terlizzi@gmsystems.com		**Chandra Gupta** **Communications & Power Industries, LLC** 516-807-9488 c.gupta@ieee.org	

G:	**Interactive Posters (all day)**	**Dipak Sengupta** **Consultant** **Analog Devices Inc., Ret.** 978-266-0061 sngdsg@gmail.com 	**Harvey Smith** **President** EMA Sales & Marketing, Inc. 508-699-4767 Harveys@imapsne.org 	**Dave Saums** **Principal** DS&A LLC 978 479 7474 dsaums@dsa-thermal.com 

45th Annual Symposium - Tuesday May 1st 2018

Afternoon Technical Program – Session Chairs

Session		Chair		Chair	
D:	Novel Packaging Applications	**Caroline Bjune** **Product Development** **Draper** 617-258-2521 cbjune@draper.com		**Mohammed Wasef** **Lead Technical Consultant** **MFR SemiTech** 908-591-5715 Mwasef@mfrsemitech.com	
E:	Interconnects	**Mike McKeown** **New Business Devel.** **Hesse-Mechatronics** 516-551-8671 michael.mckeown@hesse-mechatronics.us		**Bill Boyce** **Packaging & Process Engr.** **WBoyce Consulting** 401-523-6465 williamboyce76@gmail.com	
F:	Photonics & Optoelectronics Packaging	**Yi Qian** **MRSI Systems** 978-495-9742 yi.qian@mrsisystems.com		**Jin Li** **Sr. Product Mgr.** **Cambridge Technology** 781-266-5217 Jin.Li@cambridgetechnology.com	

Morning Session	Colonial Room
8:30 – 11:30	**Session A: MEMS** **Stephen Bart & Richard Morrison – Co-Chairs**
8:30	**"Resonant MEMS Acoustic Switch Package with Integral Tuning Helmholtz Cavity", Jonathan Bernstein**, Mirela Bancu, Douglas Gauthier, Mitchell Hansberry, John LeBlanc, Olive Rappoli, Michael Tomaino-Iannucci, Marc Weinberg - Draper, Cambridge MA
8:55	**"Nanoscale Si_3N_4 Tuning Fork Cavity Optomechanical Transducers", Rui Zhang**, Yundong Ren, Vladimir Aksyuk, Kartik Srinivasan, Yuxiang (Shawn) Liu – Worcester Polytechnic Institute,Worcester, MA
9:20	**"Electrical Yield and Reliability Issues of Ultra High Density Interposers and Update on Advanced Integration Program at BRIDG", John Allgair**, Amit Kumar, Ankineedu Velaga – BRIDG, NeoCity, FL
9:45 – 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"Development of Nanomaterial-based Smart Patches and Low-cost MEMS Devices", Cihan Yilmaz, PhD -** Flex Boston Innovation Center, Boston, MA
10:40	**"Co-fabrication of Micro-Coaxial Interconnects and Substrate Junctions for Multi-Chip Microelectronic Systems", Daniela Torres[1,2],** Anthony Kopa[1], Robert White[2], Caprice Gray[1] – [1]Draper, Cambridge, MA; [2]Tufts University, Medford, MA
11:05	**"Ion Beam Milling for MEMs Applications", James Barrett** - Ion Beam Milling, Inc., Manchester, NH
11:45 – 1:15	**Lunch & Keynote in the Exhibit Hall**

Afternoon Session	Colonial Room
1:00 – 3:05	**Session D: Novel Packaging Applications** **Caroline Bjune & Mohammed Wasef – Co-Chairs**
1:00	**"Sensor Technology Integration and Hermetic Module Fabrication Using Liquid Crystal Polymer", Susan Bagen**[1], Eckardt Bihler[2], Marc Hauer[2] - [1]Micro Systems Technologies, Inc., Lake Oswego, OR, [2]DYCONEX AG, Switzerland
1:25	**"Hybrid Electronic Construction for Wireless ECG Monitoring", Jonathan Knotts**, Vito Licata - Creative Materials, Inc., Ayer, MA
1:50	**"Gemstone – A Networkable Implantable Wireless Neurostimulator", Carlos A. Segura**, Jake G. Hellman, John R. Burns IV, Alejandro J. Miranda, Elliot Greenwald, Andrew Czarnecki, Tirunelveli S. Sriram, Matthew Muresan, Brian Nugent, Dan Guyon, Wes Uy , Caroline K. Bjune, John R. Lachapelle, and Jesse Wheeler - Draper, Cambridge, MA
2:15	**"Thermal Resistance and Effective Thermal Conductivity Measurements of Thermal Grease Using the Flash Diffusivity Method", Robert Campbell –** Netzsch Corporation, Burlington, MA
2:40	**"The Evolution of a Clinical Grade Wearable Vital Signs Monitor and the Role of Advanced Microelectronic Packaging Techniques to Increase Functionality", James Ohneck** – AEMtec/exceet North America, Cleveland / Akron, OH
3:00 – 4:30	**Refreshments, Awards, & Raffles in the Exhibit Hall**

Morning Session	Cotillion Room
8:30 – 11:30	**Session B: Printed Electronics** **Greg Fritz & Craig Armiento – Co-Chairs**
8:30	**"Applications of Metal Additive Manufacturing to Defense Electronics Systems"**, **William Villers –** TEN TECH LLC, Los Angeles, CA
8:55	**"Printed Electronics Using Magnetohydrodynamic Droplet Jetting of Molten Aluminum and Copper", Denis R. Cormier, Bruce E. Kahn,** K. Zope, D. Jayabal, and M. MedaRochester Institute of Technology, Rochester, NY
9:20	**"Printed Electronics for Aerospace and Buildings", Slade R. Culp –** United Technologies Research Center (UTRC), East Hartford, CT
9:45 – 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"Microplasma Sputtering for 3D Printing of Metallic Microstructures", Lalitha Parameswaran[1]**, Y. Kornbluth[2], R. Mathews[1], L.M. Racz[1], L.F. Velásquez-García[2,] [1]MIT Lincoln Laboratory, Lexington, MA; [2]Massachusetts Institute of Technology, Cambridge, MA
10:40	**"Printed Conductive Traces for High Power Applications by Reaction-Assisted Sintering", Sara C. Barron –** Draper, Cambridge, MA
11:05	**"Advanced Packaging for Wearables", Venkatadri Vikam –** Analog Devices Inc.,Wilmington, MA
11:45 – 1:15	**Lunch & Keynote in the Exhibit Hall**

Afternoon Session	Cotillion Room
1:00 – 3:05	**Session E: Interconnects** **Mike McKeown & William Boyce – Co-Chairs**
1:00	**"Characterization of Epoxy Cure by Dielectric Analysis (DEA)", Yanxi Zhang, PhD** – Netzsch Instruments North America LLC, Burlington, MA
1:25	**"Nano Die attach Material used in High Power Electronic Device Package", Be-Nazir Khan** – UMass Lowell, Lowell, MA
1:50	**"Wire Bonding Process: Understanding Ultrasonic Welding", Lee Levine –** Process Solutions Consulting, New Tripoli, PA
2:15	**"Multi-Dimensional Ultrasonic Copper Bonding – New Challenges for Tool Design", Paul Eichwald** - Paderborn University, Paderborn, Germany
2:40	**"Optimizing the Plasma Treatment Process Prior to Conformal Coating to Eliminate ESD Induced Failures Without Impact on Coating Performance", Trevor Zitech -** NanoBio Systems Inc., Lorain, OH
3:00 – 4:30	**Refreshments, Awards, & Raffles in the Exhibit Hall**

Morning Session	Seminar Room
8:30 – 11:30	**Session C: RF and Microwave - Innovations & Emerging Technologies** **Tom Terlizzi & Chandra Gupta – Co-Chairs**
8:30	**"High Temperature RF Multi-Layer Ceramic Capacitors (MLCC)", Brian Ward –** Vishay Americas, Shelton, CT
8:55	**"5G – The Road Ahead", Thomas Cameron, PhD** - Analog Devices Inc., Wilmington, MA
9:20	**"Automotive Example of RF Immunity Testing Shows why Full-wave Solvers Complement Challenging Measurements", Tracey Vincent** – CST [Computer Simulation Technologies], Framingham, MA
9:45 - 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"Phase Noise Origins and Measurements", Aaron Potosky,** Joe Koebel, Jason Breitibarth - Holzworth Instrumentation, Boulder, CO
10:40	**"A Heterogeneous SIP Solution for RF Applications", Justin Borski[1]**, Benjamin McMahon[2] – [1]i3 Microsystems Inc., St. Petersburg, FL; [2]BAE Systems, Merrimack, NH
11:05	**"Packaging's Role in RF and Micro-Electronics", Keith Donaldson[1]**, **Joe Spitz[2]** - [1]Intercept Technology Inc.; [2]Liberty Packaging Company, Braintree, MA
11:45 – 1:15	**Lunch & Keynote in the Exhibit Hall**

Afternoon Session	Seminar Room
1:00 – 3:05	**Session F: Photonics & Optoelectronics Packaging** **Yi Qian & Jin Li – Co-Chairs**
1:00	**"Towards an Integrated On-chip Mid-infrared Chemical Sensing System", Anuradha Agarwal -** Massachusetts Institute of Technology, Cambridge, MA
1:25	**"Integration of III-V Quantum Dot Lasers and Their Advanced Applications", Wei Guo -** University of Massachusetts Lowell, Lowell, MA
1:50	**"Lasers in Advanced Packaging", Xiangyang Song -** Cristian Porneala, Dana Sercel, Kevin Silvia, Joshua Schoenly, Rouzbeh Sarrafi, Sean Dennigan, Eric DeGenova, Scott Tompkins, Vijay Kancharla, Marco Mendes - IPG Photonics, Marlborough, MA
2:15	**"Prototype Photonic Integrated Circuits (ProtoPICs): A Flexible Platform for Hybrid Integration", Dave Kharas -** MIT Lincoln Laboratory, Lexington, MA
2:40	**"The Challenges in High Volume Manufacturing of Photonic Devices", Yi Qian -** MRSI Systems, North Billerica, MA
3:00 – 4:30	**Refreshments, Awards, & Raffles in the Exhibit Hall**

Exhibit Hall

Session G: Interactive Poster Session - Viewing All Day

Dipak Sengupta, Harvey Smith, & Dave Saums – Co-Chairs

Interactive Discussion Period: 2:00 PM – 4:00 PM

"Micro-coaxial Cable Stripping with Electronic Flame-off Process", Christian Wells[1,2], Andrew Ye[1,3]
Co-authors: Mitchell Meinhold[1], Heena Mutha[1], Caprice Gray[1], Jeffery DeLisio[1], [1]Draper, Cambridge, MA; [2]Northeastern University, Boston, MA; [3]Carnegie Mellon University, Pittsburgh, PA

"Novel Photonic Vibration Sensor for In-situ Data Acquisition", Atul Pradhan – Micatu Inc., Horseheads, NY

"Dye-Pull Inexpensive Fast Failure Analysis Technique for Solder Joints", Neeta Agarwal - Benchmark Electronics Inc., Nashua, NH

"Routing Algorithm for Complex Microelectronic Systems with Micro-Coaxial Interconnects", Austin Herrling[1,2], Michael Ricard[1], Jason Haley[1], Juan Pablo Vielma[2], Anthony Kopa[1], David Hagerstrom[1], Caprice Gray[1] – [1]Draper, Cambridge, MA; [2]Massachussetts Institute of Technology, Cambridge, MA

"Techniques to Reduce Solder Voiding Under BTC Components", Michael Johnson - MACOM Technology Solutions, Lowell, MA

"Design of Experiment Analysis of the Lid of An Electronics Package Using Finite Element Analysis", Nupur Bajad - Analog Devices Inc., Wilmington, MA

"On the Reliability of Highly Stretchable Electronic Interconnects", Ashwin V. Zachariah, M.D. Nilsson, R.S. Sivasubramony, M.D. Poliks, P. Borgesen – Binghamton University, Binghamton, NY

"On the Behavior of Ink-Jet Printed Nano Silver Traces on Porous PET Substrates in Cyclic Loading", Gurvinder Singh Khinda, Maan Kokash, Mohammed Alhendi, Jack Lombardi III – Binghamton University, Binghamton, NY

"Flexible Hybrid Electronic Circuits for Microwave Frequency Applications", Jack P. Lombardi, Yilin Sung, Mohammed Alhendi - Binghamton University, Binghamton, NY

"Soldering of Commercial BGAs and CSPs to Low Cost Flexible Substrates for Wearable Medical Monitors", Manu Yadav[1], Thaer M. Alghoul[1], Mark D. Poliks[1], Peter Borgesen[1] - [1]Binghamton University, Binghamton, NY; Luke Wentlent[2], Michael Meilunas[2] - [2]Universal Instruments, Conklin, NY

"Fatigue of Aerosol Jet Printed Interconnections on Flexible Substrates", Rajesh S. Sivasubramony, M. Alhendi, G.S. Khinda, M.Z. Kokash, J.P. Lombardi, A. Raj, D.L. Weerawarne, M. Yadav, A.V. Zachariah, M.D. Poliks, and P. Borgesen – Binghamton University, Binghamton, NY

"In Situ Functional Monitoring of Aerosol Jet-Printed Electronics", Roozbeh (Ross) Salary[1], Jack P. Lombardi[1], Darshana L. Weerawarne[2], Prahalad K. Rao[3], and Mark D. Poliks[1, 2] - [1]Department of Systems Science and Industrial Engineering,; [2]Center for Advanced Microelectronics Manufacturing, Binghamton University, Binghamton, NY; [3]Department of Mechanical and Materials Engineering, University of Nebraska-Lincoln, Lincoln, NE

"Reliability Analysis and Finite Element Modeling of a Flexible Hybrid Electronic Device", Varun Soman[1], Mark D. Poliks[1], James Turner[1], Mark Schadt[2], Michael Shay[2], Frank Egitto[2] - [1]Binghamton University, Binghamton, NY; [2]i3 Electronics Inc., Endicott, NY

"A Solder Joint Behavior Study of Extra Tall Packages by Digital Image Correlation (DIC) Method", Van-Lai Pham, Yuling Niu, Jing Wang, Huayan Wang, Shuai Shao, Charandeep Singh, Seungbae Park – Binghamton University, Binghamton, NY

"Quantification of Underfill Influence to Chip Packaging Interactions of WLCSP", Huayan Wang[1], Shuai Shao[1], Vanlai Pham[1], Panju Shang[2], Cheng Zhong[2], Seungbae Park[1] - [1]Department of Mechanical Engineering, Binghamton University, Binghamton, NY 13902 USA; [2]Huawei Technology Co. Ltd, Shenzhen, Guangdong, China

"Comprehensive Study on 2.5D Package Design for Board-Level Reliability in Thermal Cycling and Power Cycling", Shuai Shao, Yuling Niu, Jing Wang, Ruiyang Liu, Seungbae Park - Department of Mechanical Engineering, Binghamton University, Binghamton, NY

Morning Technical Program

Session A: MEMS

Chaired by Stephen Bart (TDK/InvenSense SSBC) & Richard Morrison (Draper)
Colonial Room - 8:30 AM – 11:30 AM

8:30 – 8:55 AM Colonial Room

"Resonant MEMS Acoustic Switch Package with Integral Tuning Helmholtz Cavity", Jonathan Bernstein, Mirela Bancu, Douglas Gauthier, Mitchell Hansberry, John LeBlanc, Olive Rappoli, Michael Tomaino-Iannucci, Marc Weinberg - Draper, Cambridge MA

For unattended ground sensors and the Internet of Things (IOT), wake-up sensors are needed that draw extremely low power to extend battery life. We describe in this paper a MEMS acoustic switch actuated by ambient sound pressure waves, which allows current to pass when an acoustic input at a specific frequency passes a threshold amplitude. The MEMS switch draws zero power in the absence of the target acoustic signal, and less than 10 nW when the target frequency is present. This device requires a novel package with an integral Helmholtz cavity. This cavity is designed with a threaded plunger that allows the cavity volume and the switch resonant frequency to be adjusted with 0.1 Hz accuracy.

The system uses a battery to charge a capacitor through MEMS switches activated only by the target signals. The sensor is of rotational design allowing it to be insensitive to linear vibration and static gravity forces. Analysis and experimental results demonstrating operation of these resonators in air is presented. A simple, novel fabrication process is presented which uses SOI bonded wafers and still provides metal-metal electrical contacts. These devices have successfully detected 80 Hz sound as low as 0.005 Pa RMS (48 dB SPL ref. 20 µPa) from a gas powered generator.

This work was supported by the DARPA Microsystems Technology Office N-ZERO program contract # HR0011-15-C-0138. The views, opinions, and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government. Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)

8:55 – 9:20 AM Colonial Room

"Nanoscale Si_3N_4 Tuning Fork Cavity Optomechanical Transducers", Rui Zhang, Yundong Ren, Vladimir Aksyuk, Kartik Srinivasan, Yuxiang (Shawn) Liu – Worcester Polytechnic Institute, Worcester, MA

Cavity optomechanics, which is enabled by recent development of nanofabrication technology, involves coupling between nanoscale mechanical resonators and optical cavities via radiation pressure. The optomechanical coupling enables near-field optical readout of mechanical motions with a resolution as high as sub-fm (10^{-16} m). Combined with the advantages of being batch fabricated and no alignment required, cavity optomechanical sensors provide a compact, integrated sensing platform for many applications ranging from accelerometers and gyrometers, to biological sensing.

In this work, we design, fabricate, and characterize the temperature-dependent optical and mechanical performances of a silicon nitride, nanoscale tuning fork cavity optomechanical transducer. The mechanical resonances of the tuning fork transducers can be engineered by designing the geometry of the clamp, which helps to enhance the sensitivity by achieving both high mechanical resonance frequencies (f_m) and high mechanical quality factors (Q_m). We further investigate the influence of temperature on the tuning fork. Experiment results show that f_m increased linearly with an increase of temperature. Confirmed by simulations, f_m changes were caused by 1) temperature induced Young's modules change and 2) the thermal expansion coefficient mismatch between Si and Si_3N_4. This fundamental understanding will help to design both temperature independent mechanical resonators and thermometers with high sensitivity. This work may find application when both high temporal and force resolution are important, such as those in compact sensors for atomic force microscopy.

9:20 – 9:45 AM Colonial Room

"Electrical Yield and Reliability Issues of Ultra High Density Interposers and Update on Advanced Integration Program at BRIDG", John Allgair, Amit Kumar, Ankineedu Velaga – BRIDG, NeoCity, FL

The continuing advance of Internet based activity, including mobile devices, connected sensors and cloud based operations, is driving the microelectronics industry to come up with faster devices and smaller form factors. The traditional route to CMOS miniaturization via device level scaling is reaching its limit. Our advanced integration program is aimed at developing solutions which address this challenge through innovative technologies aimed at package level scaling on a conventional silicon platform.

The Ultra High Density Interposer project is focused on developing stacked interposers with signal input/output (I/O) an order of magnitude higher than typically achieved. There are several pre and post processing challenges associated with such interposer development. This presentation will provide an analysis on the electrical yield and reliability issues of ultra high density interposers. A status overview of the advanced integration program being pursued at BRIDG will also be provided.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Colonial Room

"Development of Nanomaterial-based Smart Patches and Low-cost MEMS Devices", Cihan Yilmaz, PhD - Flex Boston Innovation Center, Boston, MA

Flex Boston Innovation Center is a concepting, design & short run production facility that supports the regional innovation economy from large multinational customers to startups. This presentation will include some of the recent work on MEMS sensors and their applications in consumer and healthcare. In the first part of the presentation, the development of a smart patch that measures accumulating lactic acid or glucose in sweat and alerts the user in real-time the chemical level will be covered. Various building blocks including the sweat sensor technology, the material and the design of a patch, the location on the body for testing, the microfluidic system concept, and the development of electrical hardware and software will be discussed. The sensor test result will also be presented.

In the second part, the design and fabrication of a low-cost ultrasonic transducer will be presented. The development of the system architecture for a transducer and system level test will be demonstrated. Several aspects of the system including the transducer material composition and availability, new fabrication techniques, and the methods for bonding multiple layers of the transducer will be discussed.

10:40 – 11:05 AM Colonial Room

"Co-fabrication of Micro-Coaxial Interconnects and Substrate Junctions for Multi-Chip Microelectronic Systems", Daniela Torres[1,2], Anthony Kopa[1], Robert White[2], Caprice Gray[1] – [1]Draper, Cambridge, MA; [2]Tufts University, Medford, MA

Micro-coaxial cables (MCCs), with outer diameter of 100µm or less, enable a new microelectronics packaging platform that will greatly reduce the time required to design and fabricate complex multi-chip microelectronic assemblies. Low-inductance MCCs for DC power and 50Ω MCCs for signals eliminate the need for lengthy simulations because each individually shielded MCC provides sufficient isolation to prevent coupling, electro-magnetic interference (EMI), and crosstalk. The in-situ fabrication method presented here utilizes only conventional wire bonding and microfabrication techniques, providing a high-feasibility path toward a new interconnect paradigm based on MCCs.

Each cable measured consists of a 25.4µm gold bond wire coated first with a dielectric and then a 5µm thick gold shield. For DC power distribution, the dielectrics evaluated are 1µm Parylene and 100nm HfO_2. Their characteristic impedances are 2.0-3.5 Ω and 0.07-0.13 Ω, respectively. A third MCC, appropriate for signals, has 38µm Parylene and a characteristic impedance of 45-52 Ω. Further characterization includes crosstalk isolation and thermal shock reliability.

11:05 – 11:30 AM Colonial Room

"Ion Beam Milling for MEMs Applications", James Barrett - Ion Beam Milling, Inc., Manchester, NH

Selective removal of material is one of the oldest methods for micromachining MEMS components, Microwave Circuits and Photonics devices. While other methods for producing these devices exist, nothing is as good as selective removal when larger quantities of parts are required. There are two primary methods of selective removal; chemical and physical.

Chemical removal (better known as etching) is a fairly old and well understood process. Materials to be etched are coated with a protective mask layer and then subjected to chemicals that etch away the undesired material. A chemical etching program is cheap and easy to set up and works well for devices with gross features. It begins to exhibit problems however when features become finer and line spacing decreases.

Ion Beam Etching is a physical process of selective removal that initially follows a similar path as Chemical Etching, but produces a better result. An anisotropic process that can produce straight sidewalls in the etched patterns and faithful reproductions of designs, it is the preferred choice for engineers whether they are manufacturing MEMS devices with line resolutions on the nanometer scale RF designers creating complex filter and coupler arrays.

This presentation will discuss the results of a recent experiment designed to quantify the actual performance differences between etch methods. A review of visual evidence will be followed by a discussion of the experimental process including the design, manufacture, and testing of sample filters using both etch methods. It will also include feedback from a customer who performed their own head to head tests comparing ion beam etching with chemical etching. The results are nothing short of extraordinary. While the actual test itself used an RF filter to demonstrate the performance differences, the application of the lessons learned to other industries such as the MEMS community will be discussed.

This presentation will also address the myth that today's Ion Beam etch process is more expensive than chemical etching. Engineers who choose Ion Beam Etching will often achieve higher quality, greater consistency and a lower cost over the inferior chemical etch process.

Lunch 11:45 – 1:15 PM in Exhibit Hall

Session B: Printed Electronics

Chaired by Greg Fritz (Draper) & Craig Armiento (UMass Lowell)

Cotillion Room - 8:30 AM – 11:30 AM

8:30 – 8:55 AM Cotillion Room

"Applications of Metal Additive Manufacturing to Defense Electronics Systems", William Villers – TEN TECH LLC, Los Angeles, CA

Additive Manufacturing, and more specifically Metal Additive Manufacturing (or Metal 3D Printing), is changing the manufacturing industry by lifting some of the design constraints inherent to traditional processes. We will present a feasibility study of a Lattice Structure created by Metal AM applied to a standard ANSI/VITA 48.2 Conduction-cooled Single Board Computer Assembly. Using a technique for which *TEN TECH LLC* holds a USPTO Provisional Patent, a 40% weight reduction was achieved while maintaining dynamics and thermal performance.

8:55 – 9:20 AM Cotillion Room

"Printed Electronics Using Magnetohydrodynamic Droplet Jetting of Molten Aluminum and Copper", Denis R. Cormier, Bruce E. Kahn, K. Zope, D. Jayabal, and M. Meda Rochester Institute of Technology, Rochester, NY

Magnetohydrodynamic (MHD) droplet jetting is a new printing technology capable of producing solid copper or aluminum conductive electronic traces. The process uses extremely inexpensive metal wire as the incoming feedstock material rather than metal powders or nanoparticle inks. Each jetted molten metal droplet partially overlaps with previously deposited material and solidifies to produce fully dense conductive metal traces whose electrical

conductivities are extremely close to those of the bulk material. The process is therefore particularly well suited for high current applications.

This talk will first present an overview of how the MHD process works. Next, practical considerations with respect to electrical conductivity, substrate compatibility, adhesion, flexural performance, and other metrics will be discussed. Lastly, the talk will look forward to applications involving fabrication of highly conductive printed electronics on non-planar surfaces and structural electronics.

9:20 –9:45 AM Cotillion Room

"Printed Electronics for Aerospace and Buildings", Slade R. Culp – United Technologies Research Center (UTRC), East Hartford, CT

The Applied Physics group at United Technologies Research Center (UTRC) is developing printed electronics methods, materials and acumen to spearhead proliferation of direct write, additive and automated high volume manufacturing methods throughout United Technologies Corporation's (UTC) business units and product offerings. UTRC and Pratt and Whitney are advancing direct write methods for in-situ measurement of critical engine parameters which previously could only be estimated. Work in novel functional materials formulation and supporting process development are enabling integrated sensing, validation and electromagnetic functionality in components across UTC Aerospace Systems in new ways which are only just beginning to be explored. High-volume, printed electronics techniques for flexible and in-mold applications are poised to transform the wearable electronics and automotive / white-good touch control industries.

The UTRC team is leveraging and evolving these techniques for implementation in buildings and aircraft environments empowering seamless manufacturing, packaging and human interactions with UTC's future products and systems. Advanced additive electronics manufacturing and packaging techniques will change the way we make and interface with our machines and UTRC is working as part of broad community to effect those changes. As a member of NextFlex (and other national manufacturing institutes), UTRC is teaming to develop autonomous printed electronics sensor platforms designed to help ensure the well-being of our people and perishable cargo.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Cotillion Room

"Microplasma Sputtering for 3D Printing of Metallic Microstructures", Lalitha Parameswaran[1], Y. Kornbluth[2], R. Mathews[1], L.M. Racz[1], L.F. Velásquez-García[2], [1]MIT Lincoln Laboratory, Lexington, MA; [2]Massachusetts Institute of Technology, Cambridge, MA

Additive manufacturing technologies promise to transform the development and production of agile microsystems, but are limited by the ability to print microelectronics-quality interconnects. State of the art 3D printing techniques for conductors cannot yet deliver the feature resolution and electrical conductivity required for high performance microcircuits, and have materials and substrate constraints, as well as post-processing requirements. We are developing a novel microplasma sputtering system that has the potential to provide direct-write capability of quality metal interconnects on non-standard substrates for integrated circuits –with future extensibility to dielectrics and semiconductors. The microplasma is generated at atmospheric pressure, obviating the need for a vacuum. By manipulating the metal at the atomic level, we retain the resistivity of bulk metal, and by sputtering the metal, we eliminate the need for post-processing or lithographic patterning.

We have modeled, designed, and constructed a first-generation atmospheric-plasma system that incorporates continuous material feed and focusing with electrostatic fields. The microplasma head has a central target wire surrounded by two pairs of electrodes, an anode pair that provides a bias to form the plasma, and a focus pair that shapes electrostatic fields to guide the ionized fraction of the working gas towards a localized spot on the substrate. The directed ions collide with sputtered metal atoms from the target dragging the metal atoms towards the substrate. This indirect electrostatic focusing mitigates the inherent spread of the sputtered material caused by collisions at atmospheric pressure, and enables fine feature definition with imprints significantly narrower than the target wire diameter. Multi-physics COMSOL simulations predict that features orders of magnitude narrower than the target-wire cross section can be printed with appropriate electric fields. We present findings from COMSOL simulations which indicate that focusing is most effective when the net normal force on the substrate is near zero, and we demonstrate printing of gold lines narrower than the target wire diameter on planar substrates.

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10:40 – 11:05 AM Cotillion Room

"Printed Conductive Traces for High Power Applications by Reaction-Assisted Sintering", Sara C. Barron – Draper, Cambridge, MA

We present a new paradigm for sintering conductive traces from a printed ink. Today's conductive ink market is dominated by inks based on silver nanoparticles that can be sintered into conductive traces by annealing at 150-200 °C for 2 hours. For certain applications, for example those requiring high currents or high temperatures, these silver-based inks are susceptible to thermally-mediated failure, such as electromigration or interdiffusion.

At Draper we are developing a new type of conductive ink that, once sintered, exhibits high temperature stability. These inks are composed of composite metal particles in a liquid carrier matrix. The composite metal particles are ball-milled particles with stored chemical energy that is released during sintering in an Intense Pulsed Light (IPL). The IPL sintering has several advantages over the thermal anneal used for nanoparticle silver inks. Firstly, the IPL's short time (3 ms) and high energy (8 J/cm^2) initiate an exothermic reaction in the metal particles, and the consequent energy release contributes local heating and sintering of the metal particles into a continuous line. We have termed this effect, "reaction assisted sintering". Secondly, the result of this reaction is a more stable material, with low susceptibility to electromigration and diffusion-related failures. Finally, the short time and inherently surface heating of IPL limits the temperature profile experienced by the substrate, and we have printed and sintered our inks on Kapton, silicon, silica, and alumina substrates. We will further describe the composite metal particles, the ink formulations, and our characterization of the conductive traces.

11:05 – 11:30 AM Cotillion Room

"Advanced Packaging for Wearables", Venkatadri Vikam – Analog Devices Inc., Wilmington, MA

The human body is very complex in nature that varies in shape and size. Our bodies expand, contract, flex and can get dirty, wet, and bumped. Conventional IC packages and boards are rectangular and are assembled using classic equipment and processes that move along Cartesian axes; side to side and up and down. There is a gap, which our industry can address. Packaging plays an important role in solving these challenges. Flexible, ergonomic and robust solutions are required to successfully implement these types of sensors and generate the accurate data that is required to maintain human health. This presentation will focus on the packaging of different sensors and signal chains onto flexible substrates and the integration of those assemblies into enclosures that will enable vital signs monitoring around the body.

These signal chains may include sensors, amplifiers, data converters, processors, RF and power management. The power management includes batteries; either disposable or rechargeable. Substrates that are flexible and comfortable, yet have the interconnect density required to bond and route among the various die and passive components, are required to enable these full signal chains. Two commonly available flex technologies are converging in this space; pattern plated and printed. Plated has the capability for fine pitch interconnect, while printed can support the cost and size requirements of, for instance, crossing our chest between ECG sensing nodes. Printed flex line & space and via technologies today don't allow the same levels of integration. There is a real opportunity for our industry here. Once a flexible substrate like this is assembled, it needs to be enclosed in materials (often textiles) that can be comfortably adhered to the skin or integrated into clothing. These materials need to maintain the ergonomic feel, while protecting the electronics from moisture and mechanical damage.

This level of integration requires advances in design and simulation tools and capabilities, new at least to IC package engineers. The complexity of packaging, variations in interconnects and often increased number of interfaces and bond layers raise reliability and FA challenges that we have not faced in conventional IC packaging. Much progress has been made, but there remains a long road ahead for our industry to enable the pervasive use of these remote vital signs monitoring sensor nodes.

Lunch 11:45 – 1:15 PM in Exhibit Hall

Session C: RF & Microwave – Innovations & Emerging Technologies
Chaired by Tom Terlizzi (GM Systems LLC) & Chandra Gupta (Communications & Power Industries, LLC)
Seminar Room - 8:30 AM – 11:30 AM

8:30 – 8:55 AM Seminar Room

"High Temperature RF Multi-Layer Ceramic Capacitors (MLCC)", Brian Ward – Vishay Americas, Shelton, CT

Today's high frequency circuits are placing increasing demands on the components they use. Tight tolerance, high quality factor and low ESR are certainly important and expected, but the requirement to operate at higher temperatures is also key. The higher operating temperature is driven by other components in the circuit such as high temperature integrated circuits and the physical location of the circuits. This paper will explore some of the applications, look at the performance characteristics of the high temperature RF capacitor, and consider how the high temperature device offers improved reliability at more mundane operating temperatures.

8:55 – 9:20 AM Seminar Room

"**5G – The Road Ahead**", **Thomas Cameron, PhD** - Analog Devices Inc., Wilmington, MA

5G is the next proposed step in the evolution of wireless networks, providing an order of magnitude improvement in bandwidth delivered to the user device and enabling new vertical businesses for mobile operators. The ultra-broadband capability envisioned for 5G is based on both a move to higher frequencies (mmwave) and the evolution of MIMO in cellular bands.

Currently there are many field trials ongoing to test the 5G proposed architectures and validate the first wave of 5G specifications. As we move forward to implement there are many challenges to be overcome by the RF and microwave design community to make 5G a reality. Will breakthroughs in mmwave technology enable a whole new cellular infrastructure, or will we see a massive deployment of massive MIMO in sub 6GHz spectrum? In many ways, the future of 5G relies on us, the RF engineering community to deliver the advanced technology of tomorrow.

Let's take this journey into the future together. During this presentation we'll start by briefly discussing the 5G industry goals and motivations. Then we'll review the technologies that are in development today enabling the early 5G radio designs and we'll highlight some of the challenges that lay ahead for the RF design community including efficient radio circuits and architectures as well as integration and packaging.

9:20 – 9:45 AM Seminar Room

"Automotive Example of RF Immunity Testing Shows why Full-wave Solvers Complement Challenging Measurements", Tracey Vincent – CST [Computer Simulation Technologies] - Framingham, MA

With increasing signaling speeds and complicated measurement set-ups Full-wave solvers are being used more and more to help design systems, investigate problems and check hypothesis. Simulation and measurement can be used separately but often can be more useful when used in synthesis. The example of RF immunity testing is taken as a test case to show why a Full-wave solver is used as the type of simulation chosen and how the measurements and simulation aid one another in helping understand the results.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Seminar Room

"Phase Noise Origins and Measurements", Aaron Potosky, Joe Koebel, Jason Breitibarth - Holzworth Instrumentation, Boulder, CO

The need to quantify the frequency stability of crystal oscillators emerged during WWII with military radar and communications systems. By the early 1970s, IEEE established the basis for the initial 1139 standard. At that point, the then slow, complex measurement was primarily used by defense systems providers and a handful of supporting

component manufacturers. With modern defense and commercial communications systems, phase noise is being rapidly adopted as the standard for verification of signal stability.

A basic oscillator circuit is presented to demonstrate where phase noise originates, along with some design considerations for improving performance. Measurement types will be further expanded to cover residual/additive as well as relating phase noise to jitter. Finally, the benefits of making phase noise measurements using a modern real time, cross correlation phase noise analyzer will be presented to demonstrate how verification of this valuable parameter has become straight forward, fast and highly accurate.

10:40 – 11:05 AM Seminar Room

"A Heterogeneous SIP Solution for RF Applications", Justin Borski[1], Benjamin McMahon[2] –[1]i3 Microsystems Inc., St. Petersburg, FL; [2]BAE Systems, Merrimack, NH

An interposer with embedded IC's has been fabricated in support of BAE Systems and Georgia Tech Research Institute using a Heterogeneous System In a Package (HSIP) technology for the purpose of creating a new and highly integrated RF MCM solution. The HSIP technology is based on well-established FOWLP (Fan-Out Wafer Level Packaging) technologies consisting of a double sided interconnect wafer fabrication process with the target IC's embedded in the HSIP interposer core. Signals are carried from front to back of the device using through-mold-via. The resulting interposer is stackable and can receive a BAE Systems MMIC die by flip chip assembly, and be subsequently stacked to a RF printed circuit main board.

In this paper, we discuss some of the key fabrication details of the HSIP device construction itself. We present an overview of selected design for manufacturability considerations, as well as the geometrical and mechanical properties of the resulting HSIP interposer devices.

11:05 – 11:30 AM Seminar Room

"Packaging's Role in RF and Micro-Electronics", Keith Donaldson[1], **Joe Spitz[2]** - [1]Intercept Technology Inc.; [2]Liberty Packaging Company, Braintree, MA

Often overlooked, packaging can and often does have significant impact on the performance of RF and Microelectronics. We will review how packaging can help protect against not only ESD damage but also EOS, caused by corrosion and oxidation of components. Corrosion can lead to increased resistance and contamination by packaging can impact performance characteristics. We will compare and contrast various packaging methods, materials and schemes, looking at benefits and drawbacks.

Lunch 11:45 – 1:15 PM in Exhibit Hall

Keynote Lunch Address

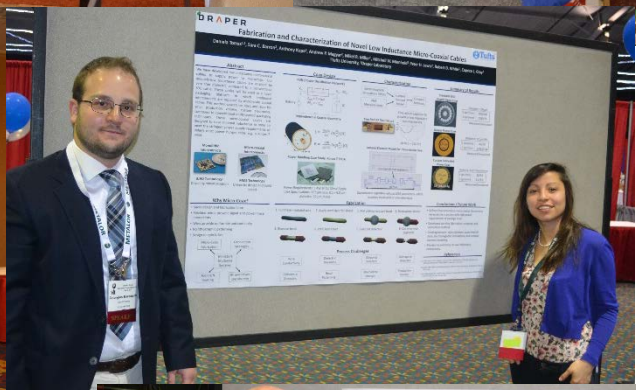
"Sensing Technologies for an Autonomous Tomorrow"

Presented by Chris Jacobs

Vice President – Analog Devices - Wilmington, MA

12:15 – Exhibit Hall

Photos of the 44th Symposium & Expo – May 2nd, 2017



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Afternoon Technical Program

Session D: Novel Packaging Applications
Chaired by Caroline Bjune (Draper) & Mohammed Wasef (MFR SemiTech)
Colonial Room - 1:00 PM – 3:30 PM

1:00 – 1:25 PM Colonial Room

"Sensor Technology Integration and Hermetic Module Fabrication Using Liquid Crystal Polymer", Susan Bagen[1], Eckardt Bihler[2], Marc Hauer[2] - [1]Micro Systems Technologies, Inc., Lake Oswego, OR, [2]DYCONEX AG, Switzerland

Innovative methods of integrating thin film manufacturing technologies known from the semiconductor industry into standard flexible substrate fabrication methods have been developed. Sputtered materials can be combined with standard copper traces to produce resistors, thermistors and thermocouples on flexible liquid crystal polymer (LCP) dielectric. These structures can be utilized for high precision temperature sensing, with thermistors providing an absolute temperature reading, while thermocouples can measure temperature differences. For example, a constantan / copper transition can measure temperature differences with a thermoelectric coefficient of 42 µV/K. Silicon sensor die, such as MEMS pressure sensors, laser-diodes or photo-diodes, can be embedded into LCP flex with cavity window openings in order to let the medium access the sensor surface. Hermetic sensor modules can also be constructed using LCP, which is a chemically and biologically stable thermoplastic polymer, having very low moisture absorption comparable to inorganic encapsulation materials such as glass. Significant miniaturization can be achieved by either embedding die into LCP flex, or utilizing LCP as a housing over standard surface mount technology (SMT) assembled components. Multilayer LCP films can be used both for the substrate and as the material for the module housing. This presentation will discuss details of the fabrication technology, examples of various module configurations including 3D forms, as well as reliability test results from extensive soak testing.

1:25 – 1:50 PM Colonial Room

"Hybrid Electronic Construction for Wireless ECG Monitoring", Jonathan Knotts, Vito Licata - Creative Materials, Inc., Ayer, MA

In this progressing digital age, the race to replace physical components with reliable virtual alternatives is in full swing, leaving devices riddled with wires looking more obsolete ever day. Most common hindrances for ECG signal quality can be ameliorated by the simple removal of wires and transition to a wireless ECG system. This presentation will compare the performance in electrode signal quality and impedance of conventional ECG electrodes with new ECG electrode materials designed for comfort.

Wireless monitoring presents challenges in creating reliable connections from a dynamic surface such as an elastic film or fabric to a rigid board and require balancing the modulus of the ink, adhesive, and encapsulant. There are many different techniques for incorporating these connections into the design which must take into consideration criteria not typical to the electronics industry such as comfort, esthetics, and skin irritation.

1:50 – 2:15 PM Colonial Room

"Gemstone – A Networkable Implantable Wireless Neurostimulator", Carlos A. Segura, Jake G. Hellman, John R. Burns IV, Alejandro J. Miranda, Elliot Greenwald, Andrew Czarnecki, Tirunelveli S. Sriram, Matthew Muresan, Brian Nugent, Dan Guyon, Wes Uy, Caroline K. Bjune, John R. Lachapelle, and Jesse Wheeler - Draper, Cambridge, MA

The neurostimulator arena is one that continues to grow and expand in capabilities as researchers and scientists find more uses and applications to deliver therapies for various conditions. As Draper attempts to jump ahead of the neurostimulators game, we've created the Gemstone – a wireless networkable implant that is not only capable of stimulation but also neural recording in all its 32 channels and contained in a volume less than 2.3cm^3. This talk will discuss the current state of the art of neurostimulators and compare the features of commercially available devices against Draper's Gemstones. The Gemstone will be described in detail from the microelectronics and packaging perspective along with the challenges and features that allows the Gemstone to potentially become the most advanced and flexible device of its kind to date.

2:15 – 2:40 PM Colonial Room

"Thermal Resistance and Effective Thermal Conductivity Measurements of Thermal Grease Using the Flash Diffusivity Method", Robert Campbell – Netzsch Corporation, Burlington, MA

Reliable performance measurements of thermal grease used as a thermal interface material in electronics packaging are important for material selection and design validation. As the grease is used in a thin layer typically 10's of microns thickness between various surfaces, measurements simulating the application can be difficult with various steady-state thermal conductivity methods. Utilizing multilayer analysis and special sample holders, the flash diffusivity method is well-suited to measurements of interfacial resistance and effective thermal conductivity of these thin interfaces. With a series of measurements over a range of grease thickness, the contact resistance and bulk thermal conductivity can also be estimated. The presentation will describe the method and sample holder setup and results for several commercially available materials will be evaluated.

2:40 – 3:05 PM Colonial Room

"The Evolution of a Clinical Grade Wearable Vital Signs Monitor and the Role of Advanced Microelectronic Packaging Techniques to Increase Functionality", James Ohneck – AEMtec/exceet North America, Cleveland / Akron, OH

Wearable devices are being used monitor a number of vital signs, such as steps, Heart rate or Energy expenditure. While these consumer targeted devices have become popular, more advanced devices are being developed and introduced that add Sleep, Stress, Blood oxygenation, Respiratory rate, Heart rate variability, Blood pulse wave, Cutaneous water / sweat and Blood glucose dynamics to the suite of monitoring parameters.

Smaller more lightweight but robust devices are viewed as less intimidating and desirable to the patient. On the other hand, practitioners such as Doctors and care givers perceive smaller devices as being more advanced technically, especially when combined with more functionality. Thus smaller more diagnostically meaningful devices are expected to increase adoption amongst healthcare professionals and their patients.

This presentation will discuss a revolutionary clinical grade vital sign monitor used for tracking Steps and Motion, Skin temperature, Heart rate, Heart rate variability, Inter-beat intervals, Blood oxygenation, Skin blood perfusion and various Scores. The methods used in the design approach to determine the optimum way to achieve the size and increased functionality requirements will be discussed as will be the microelectronic manufacturing techniques that have been and will be employed to achieve the full functionality of the device as envisioned. Further, the medical device requirements that also dictated implementation of certain functionality and technical setups will also be discussed.

Session E: Interconnects

Chaired by Mike McKeown (Hesse-Mechatronics) & William Boyce (SMART Microsystems)

Cotillion Room - 1:00 PM – 3:05 PM

1:00 – 1:25 PM Cotillion Room

"Characterization of Epoxy Cure by Dielectric Analysis (DEA), Yanxi Zhang, PhD – Netzsch Instruments North America LLC, Burlington, MA

Epoxy resin is widely used in electronic packaging industry. A variety of questions may arise during the curing process. For example, at which temperature, or after how much time, does the resin begin curing? How high is the reactivity? When is curing complete? How can the curing cycle be optimized? Is there any potential for post-curing? The answers to questions such as these can be investigated by using Dielectric Analysis (DEA), not only in the laboratory environment, but also in-process.

Dielectric Analysis (DEA) allows for the measurement of changes in the dielectric properties of a resin during curing. A sinusoidal voltage (excitation) is applied and the resulting current (response) is measured, along with the phase shift between voltage and current. These values are then used to determine the ion mobility (ion conductivity) and the alignment of dipoles. Of primary interest with regard to curing is the ion viscosity. This is the reciprocal value of the ion conductivity, which is proportional to the loss factor. Various application examples are included in the presentation.

1:25 – 1:50 PM Cotillion Room

"Nano Die attach Material used in High Power Electronic Device Package", Be-Nazir Khan – UMass Lowell, Lowell, MA

Nano material is one of the noble material for next generation high performance power electronic application. The main point of interest of the research is to use the nano silver die attach material as a hotspot thermal management package material in power electronics to achieve lower hotspot temperature, lower thermal resistance and better operating thermal performance. Nano silver die attach material used in complex power electronics hybrid packaging for silicon and SiC die attach that improves thermal conductivity, reliability, and eases manufacturability versus traditional solder paste processes.

Nano silver die attach material will be introduced as a hotspot thermal management die attach material in DCB based MOSFET package with diverse types of ICs for next generation green, complex but smaller and high-power capability electronic product to serve the purpose of the reliable power electronics.

In power electronics silicon is replaced by wide band gap semiconductor materials gallium nitride, silicon carbide because of their high thermal performance capability at elevated level of power. Nano package materials play a key role to handle the elevated temperature and power in high power integrated chips such as power MOSFETs, IGBTs. These nano materials not only suitable for high power devices but also develop the green technology trend by replacing the use of Pb-based solders in electronic ic packaging industry.

Computational fluid dynamic(CFD) based flotherm thermal modeling and simulation tool is used to develop the thermal model of power IC considering diverse types of package materials such as solder paste, epoxy, nano silver die attach material etc. Several types of package materials are compared and analyzed to develop the nano package based thermal model in power package application. Result shows the importance of nano package materials use in power product development.

1:50 – 2:15 PM Cotillion Room

"Wire Bonding Process: Understanding Ultrasonic Welding", Lee Levine – Process Solutions Consulting, New Tripoli, PA

With more than 15 trillion wire bonds produced annually and volume still growing the reliability and productivity of wire bonding makes it the dominant chip interconnection method. Estimated wire bond interconnection volume exceeds 90% of market share. But that does not mean that rigorous attention to details can be ignored. New products must be fully qualified and periodic testing of the weld intermetallic is an important part of assuring high quality bonds. Process changes, materials changes and tool changes must all be tested and reliability confirmed. Long-term aging studies using accelerated high temperature storage, thermal cycling and temperature/humidity tests are not only initial qualification requirements but should be a part of any review when materials s and encapsulation changes are required.

Wire bonding is a welding process where an intermetallic weld nugget (an alloy of the wire and the bond pad or substrate surface) is formed by the deformation of the ball or wire (wedge bonding). Ultrasonic energy unlocks easy slip mechanisms within the crystal lattice of the deforming materials allowing deformation at lower force and temperature than the materials would otherwise require for deformation. Deformation mixes the wire and substrate to form the initial bond. Subsequently diffusion allows the mixture to resolve into the equilibrium compounds of the phase diagram. The intermetallic compounds each have different physical properties and behavior. During the life of a wire bond it is normal for transformations to occur, where one intermetallic transforms to another because diffusion has increased (or decreased) the concentration of one of the elements. Transformations can generate large strains in the lattice structure, even resulting in bond failures at the interface between adjacent intermetallic compounds.

This talk will discuss the ultrasonic welding mechanism and its effect on wire bond reliability.

2:15 – 2:40 PM Cotillion Room

"Multi-Dimensional Ultrasonic Copper Bonding – New Challenges for Tool Design", Paul Eichwald - Paderborn University, Paderborn, Germany

In power electronics, copper connector pins are e.g. used to connect control boards with power modules. The new chip generation based on SiC and GaN technology increase the power density of semiconductor modules significantly with

junction temperatures reaching 200°C. To enable reliable operation at such high temperature, the soldering of these connector pins should be substituted by a multi-dimensional copper-copper bonding technology. A copper pin welded directly on DBC substrate also simplifies the assembly. With this aim, a proper bond tool and a suitable connector pin geometry are designed.

This paper presents a two-dimensional trajectory approach for ultrasonic bonding of copper pieces, e.g. connector pins, with the intention to minimize mechanical stresses exposed to the substrate. This is achieved using a multi-dimensional vibration system with multiple transducers known from flip chip bonding. Applying a planar relative motion between the bonding piece and the substrate increases the induced frictional power compared to one-dimensional excitation. The core of this work is the development of a new tool design which enables a reliable and effective transmission of the multidimensional vibration into the contact area between nail-shaped bonding piece and substrate. For this purpose, different bonding tool as well as bonding piece designs are discussed. A proper bonding tool design is selected based on the simulated alternatives. This tool is examined in bonding experiments and the results are presented. In addition, different grades of hardness for bonding piece and substrate are examined as well as different bonding parameters. Optical inspection of the bonded area shows the emergence of initial micro welds in form of a ring which is growing in direction of the interface boundaries with increasing bonding duration.

2:40 – 3:05 PM Cotillion Room

"Optimizing the Plasma Treatment Process Prior to Conformal Coating to Eliminate ESD Induced Failures Without Impact on Coating Performance", Trevor Zitech - NanoBio Systems Inc., Lorain, OH

Conformal coatings are being used more often to protect modern electronic devices from harsh environments, such as under the hood of an automobile or in the sweaty palms of an app-user's hands. It has been demonstrated that plasma treatment of such electronic assemblies can greatly enhance the adhesion of a subsequently applied conformal coating. Since plasmas are electrostatic discharges one might expect issues with damage to devices exposed to plasma. While such damage is rare there are certain sensitive electronic components that require extra care when it comes to plasma processing.

In this paper, we will present our investigative findings regarding the effects of plasma treatment prior to conformal coating. We will demonstrate the effects plasma can have on typical board components as well as ESD-sensitive components. We will also demonstrate the areas of coating adhesion, material flow characteristics and enhancement in the selectivity of the conformal coating process. The paper will share the results comparing performance on legacy printed circuit materials to high performance materials. Conformal coating materials will include acrylics, polyurethanes and silicones. The effects of plasma process parameters on conformal coating properties will also be shared.

Session F: Photonics & Optoelectronics Packaging
Chaired by Yi Qian (MRSI Systems) & Jin Li (Cambridge Technology)
Seminar Room - 1:00 PM – 3:05 PM

1:00 – 1:25 PM Seminar Room

"Towards an Integrated On-chip Mid-infrared Chemical Sensing System", Anuradha Agarwal - Massachusetts Institute of Technology, Cambridge, MA

The mid-infrared wavelength range (2.5~12μm) includes the absorption peaks of many important chemicals including environmental and industrial pollutants, toxic agents of interest to homeland security and also the medical drug delivery industry of big pharma. By analyzing the absorption spectrum of a chemical, one can (i) identify the chemical species and (ii) measure its concentration. With a Si CMOS compatible integrated mid-infrared (MIR) platform for sensing, we can envision a network of low-cost sensors for diverse applications. Here we will discuss the main building blocks of an integrated mid-infrared (MIR) sensing platform: the light source, the waveguide sensor and the detector, focusing predominantly on the development of the sensor and detector.

For both, waveguide sensor and photodetector materials, we seek (a) low-cost options with (b) low deposition temperatures for back-end Si-CMOS-compatibility, and (c) robustness against harsh sensing environments. For waveguide sensors to provide good signal to noise ratios, the material must additionally display low absorption and low sidewall scattering losses. Photodetectors must be absorptive at the wavelengths of interest.

We will discuss integration strategies for photodetectors: (i) with a sensor waveguide as well as (ii) with a resonant cavity connectorized to CMOS electronics. The detection of liquids, gases and aerosols using these devices will be discussed. Our work makes us hopeful regarding the future of mid-IR silicon photonic sensor systems.

1:25 – 1:50 PM Seminar Room

"Integration of III-V Quantum Dot Lasers and Their Advanced Applications", Wei Guo - University of Massachusetts Lowell, Lowell, MA

In this talk, we will discuss the recent work in InAs quantum dot lasers in the University of Massachusetts Lowell. Due to the three-dimension confinement in quantum dot (QD) heterostructures, InAs QDs show unique properties, such as high operation temperature and broadband emission, compared to their quantum well (QW) counterparts. It makes InAs QDs ideal candidates for several key areas. In this contest, we will discuss several applications of the quantum dot lasers, including, broad-band swept source lasers for optical coherent tomography, silicon photonics integrations for optical interconnections, parity-time symmetry laser, and topological edge state lasers. The details of the QD laser design, growth and characterizations will be discussed.

1:50 – 2:15 PM Seminar Room

"Lasers in Advanced Packaging", Xiangyang Song - Cristian Porneala, Dana Sercel, Kevin Silvia, Joshua Schoenly, Rouzbeh Sarrafi, Sean Dennigan, Eric DeGenova, Scott Tompkins, Vijay Kancharla, Marco Mendes - IPG Photonics, Marlborough, MA

Lasers are widely used for various device packaging and interconnect applications. Photonics, optoelectronics and microelectronics devices require fabrication, integration and packaging of many subcomponents from photonics integrated systems to electronics integrated systems, discrete electronics, and a variety of substrates working as carriers and interposers such as PCBs, ceramics, glass or flexible polymers. Lasers play a critical role in advancing the economics of advanced packaging while addressing requirements related to increased precision and miniaturization needs, and here we present a variety of application examples.

Lasers are used for cutting PCBs as well as metallic and ceramic frames, and can also be used for wafer level singulation of semiconductors and metals. In laser drilling different machining techniques can be used to cover a wide range of hole sizes and geometries in a variety of materials. Micromachining of complex 3D features can be done using a micro milling process whereby material removal occurs layer by layer in a controlled fashion to achieve the desired final shape to micron level accuracy. Selective laser removal can be used for creation of electrical circuits for example patterning metallic thin films on flexible polymer or rigid glass substrates. Alternatively lasers can be used to pattern away photoresist avoiding the use of expensive lithographic masks or to remove thin protective parylene coatings for local contacts. Laser lift off of thin flexible polymer films from rigid glass substrates can be used in a variety of flexible microelectronics applications. Laser marking is important for product identification, traceability and serialization and examples are provided showing how laser parameters such as wavelength and pulse duration can be chosen to match the application requirements. Finally we show examples of how laser micro welding can be used to join both metals and plastics.

2:15 – 2:40 PM Seminar Room

"Prototype Photonic Integrated Circuits (ProtoPICs): A Flexible Platform for Hybrid Integration", Dave Kharas - MIT Lincoln Laboratory, Lexington, MA

Silicon-based photonic integrated circuits (PICs) are seeing rapid adoption in datacom enabling data rates beyond 100 Gb/sec. These PICs leverage silicon (Si) waveguides operating at near-infrared wavelengths (1300-1600 nm) where Si is transparent. For photonic applications outside of telecom including lidar, bio-photonics, and atomic systems where wavelengths spanning near UV to IR are of interest, PICs based on silicon-nitride (SiN) waveguides can be utilized. Since neither Si nor SiN components emit light efficiently, light sources need to be integrated with these platforms using fiber coupling or heterogeneous integration techniques. There is a desire to combine the best-of-breed active devices (e.g., lasers, semiconductor optical amplifiers (SOAs), modulators, photodetectors) typically fabricated in III-V material systems with the Si and SiN platforms. We present a hybrid integration platform developed at Lincoln Laboratory that enables flip-chip die attach of a wide variety of III-V photonic components with our SiN PIC platform.

2:40 – 3:05 PM Seminar Room

"The Challenges in High Volume Manufacturing of Photonic Devices", Yi Qian - MRSI Systems, North Billerica, MA

Internet traffic has been growing at an exponential level, continuously driven by video streaming, 3D imaging, IoT, VR/AR, and other emerging data applications. The data generated by internet traffic is enormous and the data centers are crucial to support data communications, storage and processing through cloud computing. Photonic devices such as optical transceivers play vital roles in modern data centers. Demand for photonic devices is at an unprecedented level. And the technology upgrades are expected to happen at the same time of this volume ramp, e.g. 40G to 100G and to 200G/400G and beyond.

These requirements have posed significant challenges to photonic device manufacturing. To support data center build-up, the photonic device companies need to respond fast to data center customer's demands, and at the same time to maintain low manufacturing costs to produce profits. This calls for much higher levels of manufacturing automation than the photonic industry ever had before. In addition, the co-existence of many product standards requires that the manufacturing automation is flexible to handle high mix of products without sacrificing throughput. Furthermore, advanced technologies demand increasing precision in assembly automations, again without sacrificing speed and throughput. High speed, high precision, and high flexibility for the high volume manufacturing of photonic devices require closer collaboration than ever between device designers, process developers, manufacturing engineers, and automation equipment suppliers. We will discuss in details regarding these trends, challenges, and opportunities.

Session G: Interactive Poster Papers

Chaired by Dipak Sengupta (Analog Devices Retired), Harvey Smith (EMA), & Dave Saums (DS&A)

In Exhibit Hall – All Day Interactive Discussion Period: 2:00 – 4:00 PM

"Micro-coaxial Cable Stripping with Electronic Flame-off Process", Christian Wells[1,2], Andrew Ye[1,3],
Co-authors: Mitchell Meinhold[1], Heena Mutha[1], Caprice Gray[1], Jeffery DeLisio[1], [1]Draper, Cambridge, MA; [2]Northeastern University, Boston, MA; [3]Carnegie Mellon University, Pittsburgh, PA
The interconnect density of unshielded wires (UW) in wire-bonded circuits is limited by crosstalk and external interference. In order to surpass these limitations, micro-coaxial cables (MCCs) can be employed as interconnects in microelectronic devices. However, tensile strength limitations of MCCs limit the viability of traditional wire stripping techniques, complicating the integration of MCCs. In this work, an electronic flame-off (EFO) stripping process was investigated as a means to strip back the shield from delicate MCCs with outer diameters of 25 to 50 µm. EFO is currently used in commercial wire bonding tools as a means of forming a ball on the tip of a wire via rapid heating from a plasma discharge prior to ultrasonic bonding. This technique was used to strip back a gold shield on a polymer insulated copper wire and core-shield shorting post-EFO stripping was analyzed. High-magnification high-speed videos were taken to observe the recession of shield metal during EFO discharge. SEM analysis also confirmed that dielectric is present between the core and shield in polyimide MCCs, but absent in polyurethane MCCs after EFO stripping. The stripped end of a polyimide MCC was milled with a focused-ion-beam (FIB) and SEM showed that dielectric surrounded the core throughout its cross section. These results indicate that the decomposition temperature of the polymer insulation is a key determining factor in successful EFO stripping. In addition, a model of the EFO stripping process was developed in order to further investigate this process and determine its viability in MCCs of varying chemistries.

"Novel Photonic Vibration Sensor for In-situ Data Acquisition", Atul Pradhan – Micatu Inc., Horseheads, NY

Micatu, Inc. introduces a novel, Photonic Vibration Sensor (PHOVIS) for high performance, *in-situ* data acquisition. PHOVIS has applications, including in use as a Condition Monitoring System (CMS), for real time predictive failure analysis.

PHOVIS provides a direct optical interferometric signal measurement of vibrational displacement and frequency, in contrast to conventionally available vibration sensors. Measurement of vibrational displacement amplitudes at high resolution (sub-micron) is possible in both time series and FFT frequency data (< to 10 kHz) necessary for precise characterization of CMS signatures for wind turbines and industrial machinery. In addition, with PHOVIS there is no noise due to mechanical transfer function, thereby providing for a wide dynamic range (0.01g to 10g) and

unprecedented sensitivity and accuracy, while it is also capable of measuring transients. PHOVIS features the novel use of monolithic, solid optical components, providing a simple package and detection method in which there are no electronic components or electrical power in the sensor head making the photonic vibration sensor impervious to Radio-Frequency (RF) and Electromagnetic Interference (EMI).

Tests of PHOVIS were conducted at the National Renewable Energy Laboratory (NREL) as part of the Gearbox Reliability Collaborative (GRC) project analyzing generator disengagements to simulate grid disconnections. For these experiments, dynamometer speed decreased linearly while the drivetrain torque oscillated as it was being damped. PHOVIS installed on the gearbox monitored these events, providing real-time amplitude and spectra data, with precise (+/-1%) characterization of all transients and harmonics of the frequency signature within the sensor bandwidth.

"Dye-Pull Inexpensive Fast Failure Analysis Technique for Solder Joints", Neeta Agarwal - Benchmark Electronics Inc., Nashua, NH

With continuous miniaturization of components and increase in complex circuit card assemblies the check on integrity of hundreds of hidden joints of ball grid array and other bottom terminated components impose a challenge in X-ray and visual examinations. The assessment of Ball Grid Array (BGA) SMT joints is frequently desired in Printed Circuit Board Assembly (PCBA) industry as part of proto build assembly qualification and failure analysis investigation to minimize field risks. The "Dye and Pull" process facilitates dye penetration on fractured and separated solder joints which is visually detectable after component prying from assembly surface thus a proven viable inexpensive quick turnaround characterization method. This presentation will discuss Dye-Pull technique encompassing scope and limitations.

"Routing Algorithm for Complex Microelectronic Systems with Micro-Coaxial Interconnects", Austin Herrling[1,2], Co-authors: Michael Ricard[1], Jason Haley[1], Juan Pablo Vielma[2], Anthony Kopa[1], David Hagerstrom[1], Caprice Gray[1] - [1]Charles Stark Draper Laboratory, Cambridge, MA; [2]Massachussetts Institute of Technology, Cambridge, MA

The ability to rapidly package commercial-off-the-shelf (COTS) components 10-times faster than conventional integration strategies may be enabled by automated placement of micro-coaxial cables (MCCs) in place of standard wires or planar traces. MCCs eliminates the need for lengthy electro-magnetic simulations to evaluate interference and crosstalk and the COTS interconnects are fabricated all in 1 tool that closely resembles a conventional wire bonder. To achieve this rapid packaging strategy, we are forced to work with COTS that may or may not have I/O designed for wire bonding. Routing must also be done chip-to-chip rather than just chip-to-package resulting in a tangled "rat's nest" of interconnects. Conventional wire-routing software only routes a subset of the interconnects and does not provide solutions for wire intersections. Sequencing placement is generally computationally intractable and physical ordering of interconnect placement is often operator-defined. A direct, optimal solution can be found for complex wire-only interconnects. To evaluate feasibility of building such a system, we developed an algorithm that simultaneously evaluates the build feasibility and delivers a placement procedure. Routing feasibility is defined by the ability to place all interconnects to create a working circuit and includes parameters such as wire width, component geometries, and bonder head size. We show feasibility of routing devices with 200 and 400 interconnects and discuss how the solution depends on the limits of the developing MCC dimensions and bonding strategies. We will discuss areas of future research to achieve over 1000 MCC interconnects.

"Techniques to Reduce Solder Voiding Under BTC Components", Michael Johnson - MACOM Technology Solutions, Lowell, MA

Reducing solder voiding under BTC components is a large problem facing industry especially with the increase in the number of components being designed that require greater thermal requirements. Various techniques can be used to reduce voiding which include the design of the PCBA, the type of attachment materials used and the assembly equipment. This poster will show how the use of vias and a soldermask grid on the land pad can reduce the overall size of the voids and total voiding in solder attachment. Testing was performed using a FR4 substrate shown in Figure 1 incorporating SOT89, 3x6DFN, 4x4QFN and 5x5QFN packages. Results shown in Figures 2 and 3 show how adding the vias and the soldermask grid can influence the amount of voiding and potentially reduce the amount of voiding to less than 20%. Additional results will be provided on the use of meshed preforms to attach BTC components such as the attachment of a ceramic package directly to a heatsink and the effects of the overall stack-up on the solder attach results. The use of the meshed preforms to control the volume of solder while selecting the proper flux coating reduced the overall voiding to less than 10%. Future work on the effects of advanced heatsinking in substrate

fabrication for higher power packages will be outlined. Some of the various assembly equipment advances to help reduce solder voiding will be mentioned. Also how IPC has a document, IPC-7093 for the Design and Assembly Process Implementation for Bottom Termination SMT Components.

"Design of Experiment Analysis of the Lid of An Electronics Package Using Finite Element Analysis", Nupur Bajad - Analog Devices Inc., Wilmington, MA

A design of experiment analysis is reported on data from warpage simulations using finite element analysis of a lidded electronics package. Warpage in a lid of an optical electronics package can detrimentally affect the reliability of the package as well as its optical performance. The present study focuses on the variety of materials and designs of lids relevant to recent technologies in electronics packaging. The finite element analysis (FEA) formulation in this study accurately predicts deformation and warpage in the elastic region with optimal computational time achieved through a choice of boundary conditions and mesh sensitivity studies.

Although experimental methods provide more realistic measurements of the deformation/warpage, they may have constraints of expensive hardware, limitation over skills to operate, calibration accuracy, possibility to introduce human error. Similarly, finite element analysis method has the advantage of creating a prototype and solve under different loading conditions with less time but validation of the method is necessary and skills to operate software along with the cost to use this commercially available software. An analytical method has limitations for providing a suitable solution for all types and designs of the package. The analytical method also focuses more on estimating warpage on the mid plane of the package where as in simulation focus of the study can be associated with different components of the package. In this work, the results from FEA are compared to analytical calculations made using the classical laminate plate theory (CLPT) as well as the modified Suhir's theory. It is observed that FEA results are more accurate as they account for the performance of die attach/ under fill materials regardless of the small thickness of the layer. The FEA data is finally used to conduct a design of experiments (DOE) analysis to investigate the influence of three distinct designs and six material choices on warpage of a lid. The analysis indicates that there is no significant interaction between the two parameters expected to affect the warpage in the lid. Material properties of the lid are found to have a greater effect on the warpage of the lid as compared to variabilities introduced in lid designs in this study. The FEA simulations performed consider only material behavior within the elastic limit and in some situations, plastic deformation may occur which is more permanent and as such requires a more comprehensive analysis in the plastic region to enhance the data set for DOE studies.

This study mainly focuses on how warpage is affecting the lid deformation and techniques to characterize it. As discussed, FEA tool is used in this study to create a prototype which is similar to the actual product. The experiment is designed considering different variables such as the design of the lid and the material of the lid. Methods of the design of experiment analysis are applied to understand the correlation between these parameters. The most significant parameter in terms of the warpage deformation is addressed. Based on this study the appropriate design and material are suggested for the development of the lid over the package. This becomes helpful when there is an optoelectronic package undergoing thermomechanical loading; warpage may not only adversely affect solder joints but other parts of the package as well. So in this work, characterization of the lid of the package affected by warpage is the focus area. This study will be helpful for the development of the technologically advanced packages associated with optoelectronics.

"On the Reliability of Highly Stretchable Electronic Interconnects", Ashwin V. Zachariah, M.D. Nilsson, R.S. Sivasubramony, M.D. Poliks, P. Borgesen – Binghamton University, Binghamton, NY

Specially developed silver based inks can be screen printed onto TPU, offering inexpensive manufacturing of flexible electronics substrates that can be stretched to more than 10 times their initial length without loss of conductivity. Such stretchability is of potential interest for a broad range of applications of flexible and flexible hybrid electronics. We present results from an ongoing systematic characterization of the performance and reliability of the traces. Varying with the choice of ink the traces are not necessarily superior to alternative inkjet printed or aerosol printed ones if much more moderate levels of stretching are sufficient. Their resistances do, for example, increase much more rapidly, the resistance of one type doubling when stretched by only 2% although that one recovers completely upon unloading. Even that one is, however, damaged in repeated stretching to such levels. Comparisons between inks and to alternatives are complicated by different sensitivities to strain rates, amplitude, and holds before relaxation. Annealing and even more so exposure to humidity both tend to reduce the resistance, but this does not necessarily mean that resistance to cycling is improved, i.e. long term degradation remains a focus of ongoing studies.

"On the Behavior of Ink-Jet Printed Nano Silver Traces on Porous PET Substrates in Cyclic Loading", Gurvinder Singh Khinda, Maan Kokash, Mohammed Alhendi, Jack Lombardi III – Binghamton University, Binghamton, NY

Low cycle fatigue testing of ink-jet printed nano-Ag traces on porous PET substrates revealed an unusual behavior, the resistance ***dropping*** in cycling. The resistance would in fact increase as the substrates were stretched, and decrease again during unloading, but the resistances both at the peak strain and zero would each drop in consecutive cycles. This effect was stronger for higher strain amplitudes, but it was reduced or eliminated by preceding annealing of the samples.

The present work addresses mechanical and reliability characteristics of a Silver nanoparticle ink (Novacentrix Metalon® JS-B25HV) printed onto porous PET substrates with different roughnesses using ink-jet printing technology (FUJIFILM Dimatix-2831). Interconnects of an average width of 80 µm and two different average thicknesses (500 nm single-layer and 700 nm double-layer) were considered. Samples were subjected to different combinations of annealing and thermal cycling followed by fatigue cycling in tension and bending using an Instron-3344 tensile tester at different strain amplitudes (1.00%, 1.50% and 2.00%). The electrical resistance of each sample was monitored *in-situ* by four-point measurement.

Contact angle measurements of drops of deionized water were conducted to evaluate the roughnesses of the substrate surfaces and correlated with the test results. The change in relative resistance is faster in single layer than in double layer traces for the same strain amplitude. Cross-sections of the substrate showed pores of width ~40nm which provide good adhesion of the nano-particle ink to the substrate. We suggest that organic material infiltrating into the pores during cycling leads to a concentration of the remaining Ag on the surface and thus increasingly better connections.

"Flexible Hybrid Electronic Circuits for Microwave Frequency Applications", Jack P. Lombardi, Yilin Sung, Mohammed Alhendi - Binghamton University, Binghamton, NY

With the advent of the internet of things and distributed sensor networks, printed and flexible hybrid electronics will be key to manufacturing these devices. This is due to the fact that these sensors must be non-obtrusive and cheap, driving the adoption of printed and flexible hybrid electronics, which hold the promise of conformal mounting to objects and using cheap polymer substrates. Microwave components and structures will be needed for these sensor modules. This is because these modules will be wireless, and will need microwave components and structures for communication, among other things. As these microwave components and structures will likely be fabricated in printed and flexible hybrid electronic technologies, they must be studied and tested to assess their performance. In this study, conventional (copper plated) and printed (using aerosol jet printing) microwave structures are fabricated and compared to show differences due to the different fabrication methods. Using these results, printed antennas and more advanced microwave structures, such as a Wilkinson divider, which incorporated dispensing as well as aerosol jet printing, are fabricated and analyzed.

"Soldering of Commercial BGAs and CSPs to Low Cost Flexible Substrates for Wearable Medical Monitors", Manu Yadav[1], Thaer M. Alghoul[1], Mark D. Poliks[1], Peter Borgesen[1] - [1]Binghamton University, Binghamton, NY; Luke Wentlent[2], Michael Meilunas[2] - [2]Universal Instruments, Conklin, NY

Off the shelf Ball Grid Array (BGA) and Chip Scale Package (CSP) components are almost always offered with SnAgCu balls with either 3% or 4% Ag. Depending on the quantities required custom orders of components with another alloy may lead to major increases in price. On the other hand, most low cost flexible substrates cannot survive the process temperatures involved in SnAgCu reflow. One alternative under consideration is therefore to use a eutectic Sn-Bi solder paste. With a melting point of 139C such a paste may solder well to a contact pad with a peak reflow temperature as low as 160C. However, the partial intermixing of the alloys when soldering to SnAgCu provides for a range of properties that may vary significantly with the combination of design and process details. The consequences of this do, of course, depend on the product use conditions.

The present work focused on a flexible patient monitor to be worn in a hospital on an ongoing basis over a period of 3-5 days and then disposed of. This means that the product needs to be mechanically robust and survive low cycle fatigue, while thermal cycling is not a concern. A set of experiments was conducted to assess the effects of paste volume and reflow profiles on solder joint strength and low cycle fatigue resistance. Both strength and fatigue resistance tended to decrease with decreasing peak temperature and paste volume, but indications are that performances comparable to those of conventionally reflowed Tin-Silver-Copper solder joints can be achieved even with laser reflow and a peak temperature as low as 160C. This offers promise for the use of low cost substrates.

"Fatigue of Aerosol Jet Printed Interconnections on Flexible Substrates", Rajesh S. Sivasubramony, M. Alhendi, G.S. Khinda, M.Z. Kokash, J.P. Lombardi, A. Raj, D.L. Weerawarne, M. Yadav, A.V. Zachariah, M.D. Poliks, and P. Borgesen – Binghamton University, Binghamton, NY

The development of reliable wearable monitors that are lighter and conforming to the human body while preserving operational integrity requires among other a general understanding of the fatigue behavior of traces on flexible substrates. The present study addresses effects of tensile loading on aerosol printed AgNP (silver nano-particles) traces. These traces are nano-porous and as such inherently brittle, but the presence of a flexible substrate has major effects on their behavior and prevents the detection of changes in trace properties through direct measurement of deformation vs. the load on the trace. Studies of the evolution of damage were therefore limited to characterization of the resistance vs. variations in strain. Interpretations of results were further complicated by the time-dependent viscoelastic deformation of the substrate. Nevertheless, systematic trends are appearing.

"In Situ Functional Monitoring of Aerosol Jet-Printed Electronics", Roozbeh (Ross) Salary[1], Jack P. Lombardi[1], Darshana L. Weerawarne[2], Prahalad K. Rao[3], and Mark D. Poliks[1, 2] - [1]Department of Systems Science and Industrial Engineering,; [2]Center for Advanced Microelectronics Manufacturing, Binghamton University, Binghamton, NY; [3]Department of Mechanical and Materials Engineering, University of Nebraska-Lincoln, Lincoln, NE

Aerosol jet printing (AJP), a direct-write (DW) additive manufacturing (AM) technique, has emerged as the process of choice for the fabrication of electronics, particularly in critical applications. AJP has paved the way for high-resolution device fabrication (feature size ≤10 µm) with high placement accuracy, edge definition, and adhesion. In addition, AJP accommodates a broad range of ink viscosity (0.7–2500 cP), and allows for printing on non-planer surfaces. Despite the unique advantages and host of strategic applications, AJP is a highly unstable and complex process, prone to gradual drifts in machine behavior and deposited material. Hence, real-time monitoring and control of AJP process seem to be inevitable. The goal of this research work is *in situ* monitoring of the functional properties of aerosol jet-printed electronic devices. In pursuit of this goal, the objectives are: (i) *in situ* image acquisition from the traces of a device right after deposition; (ii) *in situ* image processing and quantification of trace morphology; and (iii) estimation of the device functional properties in a near real-time fashion. In order to address the first objective, our AJP experimental setup was sensor-instrumented, including a high-resolution charge-coupled device (CCD) camera and a variable-magnification lens to support the stranded imaging system already mounted on the AJ printer. Subsequently, following the second objective, a broad range of digital image processing algorithms was devised to quantify 2D and 3D characteristics of trace morphology, such as width, edge quality, overspray, thickness, cross-sectional area, etc. Next, to realize the third objective, a novel multiple-input, single-output (MISO) learning model was forwarded, based on sparse representation for classification (SRC). The aim is to estimate and thus monitor line resistance (a functional property) as a function of process parameters as well as trace morphology features. Finally, a computational fluid dynamics (CFD) model was developed to explain the underlying aerodynamic phenomena behind aerosol transport and deposition in AJP process, as observed experimentally. The outcomes of this research pave the way for physics-based monitoring and control of AJP process, allowing for conformal deposition of electronics with uniform functional properties.

"Reliability Analysis and Finite Element Modeling of a Flexible Hybrid Electronic Device", Varun Soman[1], Mark D. Poliks[1], James Turner[1], Mark Schadt[2], Michael Shay[2], Frank Egitto[2] - [1]Binghamton University, Binghamton, NY; [2]i3 Electronics Inc., Endicott, NY

Flexible Hybrid Electronic (FHE) devices which interface flexible substrates and sensors with conventional rigid electronic components are garnering increased attention due to their advantages of being conformal, light weight and cost efficient. These devices present a new set of reliability challenges due to their high flexibility.

We are reporting work done to improved reliability of flexible circuit of a FHE device designed to measure ECG and skin temperature. The device is fabricated on a 2" X 2" flexible Kapton® polyimide substrate of 50 µm thickness. Sensors to measure ECG and skin temperature were printed on one side of the substrate whereas conventional rigid electronic components were mounted on the other side for signal conditioning and communication purposes. The sensors were connected to the electronic components using a flexible 2 µm thick Cu circuit and Sn63Pb solder.

The device had reliability issues due to cracking of the Cu circuit near the signal conditioning chip. Multiple test vehicles were fabricated using either 2 or 6 µm thick Cu circuit, 50 or 125 µm thick polyimide substrate and either Sn63Pb or Sn42Bi solder. The aim was to determine the most reliable combination under bending loads which the device will be subjected to in real life use. The test vehicles were bend tested and optical microscopy was used to

document defects formed in the circuit and device most resistant to defect formation was determined. Cross-sectioning of defect locations was done to better understand nature of defects.

Finite element modeling was done to correlate experimental and simulation results. It was seen that both the results showed excellent correlation.

"A Solder Joint Behavior Study of Extra Tall Packages by Digital Image Correlation (DIC) Method", Van-Lai Pham, Yuling Niu, Jing Wang, Huayan Wang, Shuai Shao, Charandeep Singh, Seungbae Park – Binghamton University, Binghamton, NY

The warpage behavior at the top surface of extra tall electronic packages cannot comprehensively represent the package deformation since the considerable height change between the PCB and the component's surface. Observing the relative height change by DIC technique between the corners of the package surface and the bottom PCB is an indirect way to investigate the solder joint reliability. However, there is always a gap between those points since the shadow and blind areas caused by the light source and camera angle. In this work, an experimental study on minimizing this gap were accomplished with the digital image correlation (DIC) technique.

"Quantification of Underfill Influence to Chip Packaging Interactions of WLCSP", Huayan Wang[1], Shuai Shao[1], Vanlai Pham[1], Panju Shang[2], Cheng Zhong[2], Seungbae Park[1] - [1]Department of Mechanical Engineering, Binghamton University, Binghamton, NY 13902 USA; [2]Huawei Technology Co. Ltd, Shenzhen, Guangdong, China

The underfill selection and its fillet formation influence to the Chip Packaging Interactions(CPI) of WLCSP was investigated through an experimental technique and numerical analysis. For the experimental assessment, thermo-mechanical interactions between die corner and underfill was investigated. Digital image correlation (DIC) technique with optical microscope was utilized to quantify the deformation behavior and strains of cross-sectioned WLCSP die corner subjected to thermal loading from 25˚C to 125˚C. Finite element analysis(FEA) was conducted by simulating the thermal loading applied in the experiments, and validated with experimental results.

"Comprehensive Study on 2.5D Package Design for Board-Level Reliability in Thermal Cycling and Power Cycling", Shuai Shao, Yuling Niu, Jing Wang, Ruiyang Liu, Seungbae Park - Department of Mechanical Engineering, Binghamton University, Binghamton, NY

2.5D packages have been widely used in electronics industry for high performance and product miniaturization. As Through-Silicon-Via (TSV) fabrication methods and multi-level assembly technologies get mature, 2.5D packaging becomes reliable and affordable. In this work, board-level life prediction was performed for a 2.5D Field-Programmable Gate Array (FPGA) assembly in both accelerated thermal cycling (ATC) and power cycling (PC). Finite element models were built and validated by warpage measurement. Solder fatigue life in PC was investigated by computational fluid dynamics (CFD) simulation and finite element analysis. Improved life prediction for PC was achieved by mapping temperature results from CFD model to finite element model.

Exhibits *** Exhibits *** Exhibits

Student Presentation Awards, Refreshments, Hors d'oeuvres, Raffles, & Fun in the Exhibit Hall Until 4:30 PM

International Microelectronics Assembly and Packaging Society
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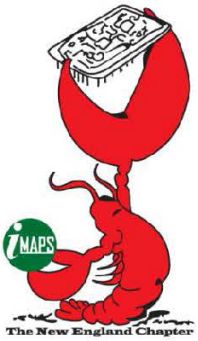

May 7th, 2019

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The New England Chapter Symposium Technical Program Committee seeks papers that demonstrate how new technologies and applications are expanding and redefining microelectronics. Areas of interests include:

Industry	Advanced Processes & Materials
• Biomedical Electronics • Telecom - Microwave • Military Electronics • Consumer Electronics • Renewable Energy: Fuel Cells, Solar, Wind • Thermal Management • Manufacturing, Outsourcing & Quality • Solar/PV • High Performance Interconnects and Boards • Imaging Sensors • Emerging Technologies	• 2.5 / 3D and High Density Packaging • Photonic / Optoelectronic Packaging • LED Packaging • MEMS and Nano Packaging • Underfill, Encapsulants, and Adhesives • Green Packaging / Compliance with RoHS • Flip-Chip and Bumping: Processes, Reliability • Wirebonding and Stud Bumping • Embedded and Integrated Passives • Ceramic, Polymer and Conductive Materials • Conformal Electronic Materials • Wearable / Printed Electronics

Please send 250 word abstract to Dmitry Marchenko – dmarchenko@gmail.com
Or Send to: Abstracts@imapsne.org

Submission form and more details available at - www.imapsne.org

Deadline for Abstract Submission – December 31, 2018

¿MAPS New England Technical Meeting & Chapter Business Meeting

June 19, 2018

Holiday Inn Hotel & Suites, Marlborough, MA
265 Lakeside Ave., Marlborough, MA 01752

"Prototype Photonic Integrated Circuit (ProtoPIC) Platform and Applications"

Dr. Dave Kharas, Member of the Technical Staff,
MIT Lincoln Laboratory, Lexington, MA

Summary : Silicon-based photonic integrated circuits (PICs) are seeing rapid adoption in datacom, enabling data rates beyond 100 Gb/sec. These PICs leverage silicon (Si) waveguides operating at near-infrared wavelengths (1300-1600 nm) where Si is transparent. For photonic applications outside of telecom including lidar, bio-photonics, and atomic systems where wavelengths spanning near UV to IR are of interest, PICs based on silicon-nitride (SiN) waveguides can be utilized. Since neither Si nor SiN components emit light efficiently, light sources need to be integrated with these platforms using fiber coupling or heterogeneous integration techniques. There is a desire to combine the best-of-breed active devices (e.g., lasers, semiconductor optical amplifiers (SOAs), modulators, photodetectors) typically fabricated in III-V material systems with the Si and SiN platforms. We present a hybrid integration platform that enables flip-chip die attach of a wide variety of III-V photonic components with our SiN PIC platform. This technology can be leveraged to benefit a variety of photonic applications that are being developed at Lincoln Laboratory.

Speaker: Dr. Kharas is a member of the Quantum Information and Integrated Nanosystems Group at Lincoln Laboratory, where he is working in the Integrated Photonics Team in a process integration role. Dr. Kharas leads the Photonics Team's device fabrication activities across a number of technology platforms including silicon and nitride PICs, hybrid integration of III-V components, MEMS and Microfluidic devices. Prior to joining Lincoln Labs, Dr. Kharas led the AlInGaP Technology Group at Philips Lumileds. He holds PhD and MS degrees in Materials Science from SUNY Stony Brook, and a BS in Applied Physics from UMASS Lowell.

SCHEDULE (times approximate)

5:30 PM	**Registration, Socializing, Networking & Cash Bar**
6:30 PM	**Dinner**
7:15 PM	**Annual Business Meeting & Elections – Jon Medernach, President**
	The Chapter Nominating Committee presents the following slate of Officer Candidates for the 2018-2019 Term:
	President - Dmitry Marchenko, BAE
	Vice-President - Matt Bracy, MSD
	Treasurer - Jeremy Lug, Metrigraphics
7:30 PM	**Technical Presentation - Dr. Dave Kharas**

You may attend the presentation without eating dinner. Pre-Registration deadline is Wednesday, June 13..!!! After that, or for Walk-Ins At-Door, the fee is an additional $5.00 [Limited Availability].
Cancellations must be received by 3:00 p.m. Monday 6/18... or The Chapter will bill you for the registration fee. Options: To cancel a registration or register by e-mail, contact Matt Bracy: matt@msdsales.com

INFORMATION & REGISTRATION - at www.imapsne.org/ChapterMeetings.php

iMAPS New England

46th Annual Symposium & Expo

May 7, 2019 - Boxboro Regency Hotel & Conference Center

THEME: *TBD*

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For more info contact Exhibits Chair, Michael Toro, AMETEK AEGIS, Michael.Toro@ametek.com (508) 425-6917

Remember to make frequent visits to our website: www.imapsne.org

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